CLAIMS

What is claimed is:

1. A printer, comprising:

(a) a first address bus;

(b) a second address bus;

(c) an address translation unit (ATU), coupled to the first and second address buses, operable to translate virtual addresses received from at least two bus masters connected to the first bus into physical memory addresses.

2. The printer of claim 1, wherein the ATU is further operable to transmit the physical address over the second bus.

3. The printer of claim 2, further comprising:

(d) a print engine coupled to the first address bus.

4. The printer of claim 3, further comprising:

(e) a central processing unit (CPU) coupled to the first address bus.

5. The printer of claim 4, further comprising:

(f) a DMA controller coupled to the first address bus.

6. The printer of claim 5, further comprising:

(g) a memory coupled to the second address bus.

7. The printer of claim 6, wherein the CPU and the DMA controller are both operable to transmit virtual addresses to the ATU over the first address bus.

8. The printer of claim 7, wherein the ATU is operable to translate the virtual addresses received from the CPU controller and the DMA

controller into physical addresses for addressing the memory and to then transmit these physical addresses to the memory over the second address bus.

9. A printer , comprising:

(a) a DMA controller operable to generate virtual addresses;

(b) a CPU operable to generate virtual addresses; and

(c) an address translation unit operable to receive the virtual addresses from both the DMA controller and the CPU and to translate the virtual addresses into physical addresses.

10. The printer of claim 9, further comprising:

(d) a memory coupled to the address translation unit.

11. The printer of claim 10, wherein the address translation unit is operable to transmit the physical addresses to the memory.

12. The printer of claim 11, further comprising:

(e) a virtual memory bus; and

(f) a physical bus; and

(g) wherein the DMA controller and the CPU is coupled to the virtual memory bus and the memory is coupled to the physical bus and the address translation unit is coupled to both the virtual memory bus and the physical memory bus.

13. The printer of claim 12, further comprising:

(h) a print engine coupled to the virtual memory bus.

14. In a printer, including a CPU, a DMA controller, and a memory, method of generating physical addresses for the memory, comprising:

(a) providing an address translation unit (ATU);

(b) the CPU transmitting a first plurality of virtual addresses to the ATU; and

(c) the DMA controller transmitting a second plurality of virtual addresses to the ATU.

15. The method of claim 14, further comprising

(d) the ATU generating physical addresses from the virtual addresses received from the CPU.

16. The method of claim 15, further comprising:

(e) the ATU generating physical addresses from the virtual addresses received from the DMA controller.

17. The method of claim 16, further comprising:

(f) The ATU transmitting the physical addresses generated in step (d) to the memory.

18. The method of claim 16, further comprising:

(f) the ATU transmitting the physical addresses generated in step (e) to the memory.

19. A computer, comprising:

(a) a DMA controller;

(b) a CPU; and

(c) an address translation unit operable to receive virtual addresses from both the DMA controller and the CPU and to translate the virtual addresses into physical addresses.

20. The computer, further comprising:

(d) a memory coupled to the address translation unit; and wherein the address translation unit is operable to transmit the physical addresses to the memory.